Amendments to the Claims:

11. (Currently amended) An I/C chip suitable for wire bonding comprising:

at least one conductive bond pad;

at least one layer of dielectric material overlying said conductive bond pad;

a surface defining an opening in said layer of dielectric material exposing said conductive bond pad; ~~and~~

a conductive seed layer disposed in said opening ~~at least one layer of conductive material~~ overlying said conductive bond pad and in contact therewith and in contact with the entire surface of said opening and having at least one exposed edge; and ~~also overlying and in contact with the entire surface of said opening~~

at least one layer of said conductive material overlying said conductive seed layer and completely covering said conductive seed layer including all exposed edges.

12. (Currently amended) The ~~invention~~ I/C chip as defined in claim 11 wherein there are two layers of conductive material plated on said conductive seed layer ~~bond pad~~ in said opening.

13. (Currently amended) The ~~invention~~ I/C chip as defined in claim 12 wherein said two layers of conductive material are Ni and Au.

14. (Canceled)

15. (Currently amended) The ~~invention~~ I/C chip as defined in claim 14 wherein an intermediate conductive layer is provided between said conductive seed layer and said conductive bond pad.

16. (Currently amended) The ~~invention~~ I/C chip as defined in claim 15 wherein the intermediate conductive layer is TaN/Ta.

17. (Currently amended) The ~~invention~~ I/C chip as defined in claim 11 wherein the conductive bond pad in the I/C chip is Al.

18. (New) The I/C chip as defined in claim 11 wherein said at least one layer of conductive material defines a wall in said I/C chip in which is disposed a ball bond and wire.

19. (New) The I/C chip as defined in claim 18 wherein the ball bond is Au.